Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1. (currently amended) An integrated circuit comprising a high voltage transistor on a semiconductor, the high voltage transistor comprising:

a source formed in the semiconductor;

a drain formed in the semiconductor; and

a channel between the source and the drain,

wherein the drain comprises a first drain extension region, a second drain extension region, and a third drain region, a concentration of majority charge carriers in the drain increasing farther away from the channel at junctions between the three drain regions,

wherein the drain further comprises a first doped well that overlaps the first drain extension region, the first doped well having a first concentration of dopant that reduces majority carriers in the first drain extension region, and

wherein the drain further comprises a second doped well that overlaps the second drain extension region, the second doped well having a second concentration of dopant that reduces majority carriers in the second drain extension region.

Claim 2. (original) The integrated circuit of claim 1, further comprising:

a gate formed in a ring structure that encloses the drain.

Claim 3. (original) The integrated circuit of claim 1, further comprising:

a gate formed into a striped structure.

Claim 4. (original) The integrated circuit of claim 1, further comprising:

a gate shield formed partially over a gate and the drain.

Claim 5. (original) The integrated circuit of claim 1 wherein the drain further comprises:

a fourth drain region adjacent to the third drain region that has a concentration of majority charge carriers that is greater than the concentration of majority charge carriers in the first, second, and third drain regions, and wherein the third drain region is a third drain extension region.

Claim 6. (original) The integrated circuit of claim 5 further comprising:

a fifth drain region adjacent to the fourth drain region that has a concentration of majority charge carriers that is greater than the concentration of majority charge carriers in the first, second, third, and fourth drain regions, wherein the fourth drain region is a fourth drain extension region.

Claim 7. (currently amended) ~~The integrated circuit of claim 1 further comprising:~~

An integrated circuit comprising a high voltage transistor on a semiconductor, the high voltage transistor comprising:

a source formed in the semiconductor;

a drain formed in the semiconductor;

a channel between the source and the drain, wherein the drain comprises a first drain extension region, a second drain extension region, and a third drain region, a concentration of majority charge carriers in the drain increasing farther away from the channel at junctions between the three drain regions;

a first doped well;

the first drain extension region comprising a region where part of the first doped well overlaps part of a first doped region;

a second doped well; and

the second drain extension region comprising a region where part of the second doped well overlaps part of the first doped region.

Claim 8. (original) The integrated circuit of claim 7 further comprising:

a third doped well;

the third drain region comprising a third extension region formed where part of the third doped well overlaps part of the first doped region; and

a fourth drain region that comprises a low resistance drain contact region.

Claim 9. (original) The integrated circuit of claim 7 further comprising:

a third doped well;

the third drain region comprising a third extension region formed where part of the third doped well overlaps part of the first doped region;

a fourth drain extension region; and

a fifth drain region that comprises a drain contact region.

Claim 10. (original) The integrated circuit of claim 9 further comprising:

a fourth doped well;

the fourth drain extension region formed where a portion of the fourth doped well overlaps part of the first doped region.

Claim 11. (original) The integrated circuit of claim 8 wherein,

P-type dopant is diffused into the first doped well,

P-type dopant is diffused into the second doped well,

N-type dopant is diffused into the third doped well, and

N-type dopant is diffused the first doped region.

Claim 12. (currently amended) A high voltage transistor formed on a semiconductor, the transistor comprising:

a gate formed on the semiconductor;

a source formed in the semiconductor; and

a drain formed in the semiconductor, ~~wherein the drain comprises at least four doped drain regions,~~

~~the four doped drain regions having a gradient of majority charge carriers that laterally increases farther away from the gate across three junctions between the four drain regions~~

wherein the drain comprises a first drain extension where the drain overlaps a first doped well, and a second drain extension where the drain overlaps a second doped well, and dopants that form the first and the second doped wells reduce majority carriers in the drain, and

wherein a gradient of majority carriers laterally increases farther away from the gate across the first drain extension, the second drain extension, and a third drain region.

Claim 13. (currently amended) ~~The high voltage transistor of claim 12~~
A high voltage transistor formed on a semiconductor, the transistor comprising:
a gate formed on the semiconductor;
a source formed in the semiconductor; and
a drain formed in the semiconductor, wherein the drain comprises at least four doped drain regions,

the four doped drain regions having a gradient of majority charge carriers that laterally increases farther away from the gate across three junctions between the four drain regions,

wherein a first drain extension region comprises a portion of a first well that overlaps a first doped region,

a second drain extension region comprises a portion of a second well that overlaps the first doped region,

a third drain extension region comprises a portion of the first doped region; and
a fourth drain region comprises a drain contact region.

Claim 14. (original) The high voltage transistor of claim 13 wherein the third drain region comprises a portion of a third well that overlaps the first doped region.

Claim 15. (original) The high voltage transistor of claim 13 wherein,
P-type dopant is diffused into the first well,

P-type dopant is diffused into the second well, and

N-type dopant is diffused the first doped region.

Claim 16. (currently amended) The high voltage transistor of claim 12 A high voltage transistor formed on a semiconductor, the transistor comprising:

a gate formed on the semiconductor;

a source formed in the semiconductor; and

a drain formed in the semiconductor, wherein the drain comprises at least four doped drain regions,

the four doped drain regions having a gradient of majority charge carriers that laterally increases farther away from the gate across three junctions between the four drain regions,

wherein the drain further comprises:

a first drain extension comprising a portion of a first well that overlaps a first doped region,

a second drain extension comprising a portion of a second well that overlaps the first doped region,

a third drain extension comprising a portion of a third well that overlaps the first doped region;

a fourth drain extension region; and

a fifth drain region that comprises a drain contact region.

Claim 17. (currently amended) An integrated circuit comprising at least one high voltage transistor formed on a semiconductor, said transistor comprising:

a source formed in the semiconductor; and

a drain formed in the semiconductor, wherein the drain comprises a first potion of a first doped region that overlaps a first doped well, a second portion of the first doped region that overlaps a second doped well, and a drain contact region, and wherein dopants that form the first doped well reduce majority carriers in the first portion of the first doped region, and dopants that form the second doped well reduce majority carriers in the second portion of the first doped region.

Claim 18. (currently amended) ~~The integrated circuit of claim 17~~ An integrated circuit comprising at least one high voltage transistor formed on a semiconductor, said transistor comprising:

a source formed in the semiconductor; and

a drain formed in the semiconductor, wherein the drain comprises a first potion of a first doped region that overlaps a first doped well, a second portion of the first doped region that overlaps a second doped well, and a drain contact region,

wherein the drain further comprises a third portion of the first doped region that overlaps a third doped well, wherein the third portion of the first doped region has a concentration of majority carriers that is greater than the concentration of majority carriers in the first and the second portions of the first doped region.

Claim 19. (original) The integrated circuit of claim 18 wherein the drain further comprises a fourth portion of the first doped region that overlaps a fourth doped well, wherein the fourth portion of the first doped region has a concentration of majority carriers that is greater than the concentration of majority carriers in the third portion of the first doped region.

Claim 20. (currently amended) The integrated circuit of claim 17 wherein the transistor is an NMOS transistor,

the first doped region of the drain is doped with N-type dopant,

the first doped well is doped with P-type dopant, and

the second doped well is doped with ~~N-type~~ P-type dopant.

Claim 21. (currently amended) ~~The integrated circuit of claim 17~~ An integrated circuit comprising at least one high voltage transistor formed on a semiconductor, said transistor comprising:

a source formed in the semiconductor; and

a drain formed in the semiconductor, wherein the drain comprises a first potion of a first doped region that overlaps a first doped well, a second portion of the first doped region that overlaps a second doped well, and a drain contact region,

wherein the drain further comprises:

a third portion of the first doped region that overlaps a third doped well, and

wherein the concentration of majority charge increases across junctions between the three portions of the first doped region moving laterally away from a gate of the transistor.

Claim 22. (original) The integrated circuit of claim 21 wherein the drain further comprises:

a fourth portion of the first doped region, and

wherein the concentration of majority charge increases across junctions between the four portions of the first doped region moving laterally away from a gate of the transistor.

Claim 23. (original) The integrated circuit of claim 17 wherein the transistor is an NMOS or a PMOS device.

Claim 24. (currently amended) ~~The integrated circuit of claim 17~~

An integrated circuit comprising at least one high voltage transistor formed on a semiconductor, said transistor comprising:

a source formed in the semiconductor; and

a drain formed in the semiconductor, wherein the drain comprises a first potion of a first doped region that overlaps a first doped well, a second portion of the first doped region that overlaps a second doped well, and a drain contact region,

wherein a concentration of majority charge carriers increases laterally away from a channel of the transistor across junctions between each doped region of the drain.

Claim 25. (original) A high voltage transistor formed on a semiconductor, the transistor comprising:

a gate formed on the semiconductor;

a source formed in the semiconductor; and

a drain formed in the semiconductor, wherein the drain region has a graded concentration of first majority charge carriers that increases across junctions between a first drain extension, a second drain extension, and a third drain region moving laterally farther away from the gate, and

wherein a concentration of second charge carriers in a region beneath the drain decreases moving laterally farther away from the gate to underneath the third drain region, the second charge carriers being of the opposite doping type as the first majority charge carriers.

Claim 26. (original) The high voltage transistor of claim 25 further comprising:

a first doped well;

the first drain extension comprising a region where part of the first doped well overlaps part of a first doped region;

a second doped well; and

the second drain extension comprising a region where part of the second doped well overlaps part of the first doped region.

Claim 27. (original) The high voltage transistor of claim 26 further comprising:

a third doped well;

the third drain region comprising a third drain extension region formed where part of the third doped well overlaps part of the first doped region;

a fourth drain extension region; and

a fifth drain region that comprises a drain contact region.

Claim 28. (original) The high voltage transistor of claim 25 wherein the third drain region comprises a low resistance drain contact region.

Claim 29. (original) The high voltage transistor of claim 26 further comprising:

a third doped well;

the third drain region comprising a third drain extension formed where part of the third doped well overlaps part of the first doped region; and

a fourth drain contact region.